CLAIMS

What is claimed is:

1. A method of communicating a plurality of parallel data packets from a first data parallel bus to a second parallel data bus, comprising the steps of:
   a. separating each of the plurality of parallel data packets into a first portion and a second portion;
   b. converting each first portion into a first serial data stream and converting each second portion into a second serial data stream;
   c. transmitting the first serial data stream over a first serial data channel and transmitting the second serial data stream over a second serial data channel;
   d. converting the first serial data stream into a plurality of first received portions and converting the second serial data stream into a plurality of second received portions; and
   e. combining selected first received portions with corresponding selected second received portions so as to regenerate the plurality of parallel data packets.

2. The method of Claim 1, wherein the first serial data channel and the second serial data channel each comprise an optical serial data link.

3. The method of Claim 1, further comprising the step of receiving data using a plurality of FIFO's, each FIFO having a read side and a write side.

4. The method of Claim 3, further comprising the step of executing an error-recovery state machine comprising the steps of:
   a. entering a first write state when either a write side error signal or a read initialization request signal is asserted and performing the following operations:
      i. writing to all FIFO's is stopped; and

ii. a write initialization request signal is asserted;

b. exiting the first write state when an initialization signal is asserted,

c. entering a second write state from the first write state and de-asserting a write side initialization request signal;

d. exiting the second write state when the initialization signal is de-asserted;

e. entering a third write state from the second write state and resuming normal operations;

f.. entering a first read state when either read side error signal or a write side initialization request signal is asserted, and performing the following operations:

i. reading from all FIFO's is stopped; and

ii. a read initialization request signal is asserted;

g. exiting the first read state when all initialization request signals are asserted,

h. entering a second read state from the first read state and performing the following operations:

i. asserting the initialization signal; and

ii. de-asserting the read initialization signal;

i. exiting the second read state when all initialization request signals are de-asserted; and

j. entering a third read state from the second read state and de-asserting the initialization signal.

5. The method of Claim 4, wherein the plurality of FIFO's include a first A-FIFO, a second A-FIFO, a first B-FIFO and a second B-FIFO, the method further comprising the step of executing the following operation while in the second write state of one second FIFO: asserting an additional request signal from one of the second FIFO's to the first FIFO's.

6. The method of Claim 5, further comprising the step of executing the following operation while in the third write state of one of the second

FIFO's: de-asserting the additional initialization request signal in the second FIFO.

7. The method of Claim 5, wherein each of the A-FIFO's and B-FIFO's include a FIFO fullness indicator and further comprising the step of consuming a first predetermined character when the FIFO fullness indicator for a FIFO indicates that the FIFO fullness is greater than a first predetermined threshold.

8. The method of Claim 7, further comprising the step of generating a second predetermined character when the FIFO fullness indicator for a FIFO indicates that the FIFO fullness is less than a second predetermined threshold.

9. The method of Claim 8, wherein the second predetermined character comprises a unique character that is recognized only as a generated character.

10. An apparatus for transmitting a plurality of data words from a first parallel data bus to a second parallel data bus, comprising:

a. a first serializer, in data communication with the first parallel bus, that transforms a first portion of each data word into a first serial data stream;

b. a second serializer, in data communication with the second parallel bus, that transforms a second portion, different from the first portion, of each data word into a second serial data stream;

c. a first serial data channel, in data communication with the first serializer, upon which the first serial data stream may be transmitted;

d. a second serial data channel, in data communication with the second serializer, upon which the second serial data stream may be transmitted;

e. a first de-serializer, in data communication with the first serial data channel, that transforms the first serial data stream into a plurality of first parallel data units, each first parallel data unit being identical to a corresponding first portion of a data word;

f. a second de-serializer, in data communication with the second serial data channel, that transforms the second serial data stream into a plurality of second parallel data units, each second parallel data unit being identical to a corresponding second portion of a data word; and

g. a receiver element that receives the first parallel data units from the first de-serializer and the second parallel data units from the second de-serializer and that assembles corresponding ones of the first parallel data units and the second parallel data units into corresponding data words and that transmits the corresponding data words to the second parallel data bus.

11. The apparatus of Claim 10, wherein the receiver element comprises:

a. a first A-FIFO that is capable of receiving data from the first de-serializer;

b. a first B-FIFO that is capable of receiving data from the second de-serializer;

c. a second A-FIFO that is capable of receiving data from the first A-FIFO;

d. a second B-FIFO that is capable of receiving data from the first B-FIFO; and

e. a logic element that concatenates data from the second A-FIFO with data from the second B-FIFO to generate a data word and that transmits the data word to the second parallel data bus.

12. The apparatus of Claim 11, wherein the first A-FIFO has a write side and wherein the write side of the first A-FIFO is clocked by an a-channel clock extracted from the first de-serializer.

13. The apparatus of Claim 11, wherein the first B-FIFO has a write side and wherein the write side of the first B-FIFO is clocked by a b-channel clock extracted from the second de-serializer.

14. The apparatus of Claim 11, wherein the first A-FIFO has a read side and the first B-FIFO has a read side and wherein the read sides of both the first A-FIFO and the first B-FIFO are clocked by a common reference clock.

15. The apparatus of Claim 11, wherein the second A-FIFO and the second B-FIFO each have a write side and wherein the write sides of both the second A-FIFO and the second B-FIFO are clocked by a common reference clock.

16. The apparatus of Claim 11, wherein the second A-FIFO and the second B-FIFO each have a read side and wherein the read sides of both the second A-FIFO and the second B-FIFO are clocked by a common system clock.

17. The apparatus of Claim 11, further comprising a error recovery logic element that embodies a state machine that includes the following elements:

a. a first write state, which is entered when either a write side error signal or a read initialization request signal is asserted, which exited when an initialization signal is asserted, and in which the following operations are performed:
   i. writing to all FIFO's is stopped; and
   ii. a write initialization request signal is asserted;

b. a second write state, which is entered from the first write state, which is exited when the initialization signal is de-asserted, and in which a write side initialization request signal is de-asserted;

c. a third write state, which entered from the second write state and in which normal operations are resumed;

d. a first read state which is entered when either read side error signal or a write side initialization request signal is asserted, which is

exited when all initialization request signals are asserted, and in which the following operations are performed:

i. reading from all FIFO's is stopped; and

ii. a read initialization request signal is asserted;

e. a second read state, which is entered from the first read state, which is exited when all initialization request signals are de-asserted, and in which the following operations are performed:

i. the initialization signal is asserted; and

ii. the read initialization request signal is de-asserted; and

f. a third read state, which is entered from the second read state and in which the initialization signal is de-asserted.

18. The apparatus of Claim 17, wherein the following operation is further performed in the second write state: asserting an additional request signal from one of the second FIFO's to the first FIFO's.

19. The apparatus of Claim 17, wherein the following operation is further performed in the third write state: de-asserting the additional initialization request signal in the second FIFO.

20. The apparatus of Claim 11, wherein each of the A-FIFO's and B-FIFO's include a FIFO fullness indicator and wherein each of the A-FIFO's and B-FIFO's includes a first logic element that consumes a first predetermined character when the FIFO fullness indicator for a FIFO indicates that the FIFO fullness is greater than a first predetermined threshold.

21. The apparatus of Claim 20, wherein each of the A-FIFO's and B-FIFO's includes a second logic element that generates a second predetermined character when the FIFO fullness indicator for a FIFO indicates that the FIFO fullness is less than a second predetermined threshold.

22. The apparatus of Claim 21, further comprising a circuit that recognizes a fill character anywhere in an incoming data stream and that removes the fill character from the incoming data stream.

23. The apparatus of Claim 20, wherein the second predetermined character comprises a unique character that is recognized only as a generated character.

24. The apparatus of Claim 10, further comprising:

a. a central FIFO; and

b a read-side logic element that detects at least one of the following: a lack of a sync character, or an irregularity in a clock frequency.

25. The apparatus of Claim 10, further comprising a circuit element that periodically and contemporaneously adds to both the first serial data stream and the second serial data stream an alignment character.